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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,895	08/31/2001	Sung-Chul Han	678-629 (P9648/ST2)	2073
28249	7590	10/05/2005	EXAMINER	
DILWORTH & BARRESE, LLP 333 EARLE OVINGTON BLVD. UNIONDALE, NY 11553			TABONE JR, JOHN J	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/943,895

Applicant(s)

HAN, SUNG-CHUL

Examiner

John J. Tabone, Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,7 and 9-12 is/are rejected.
- 7) ☐ Claim(s) 6 and 8 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **FINAL DETAILED ACTION**

1. Claims 1-12 are pending in the application and have been examined. Claims 1-5, 7 and 9-12 remain rejected. Claims 6 and 8 remain objected to as allowable subject matter.
2. Examiner withdraws the objection to claim 10 as a result of Applicant's amendment filed 07/11/2005.

### ***Response to Arguments***

3. Applicant's arguments filed 07/11/2005 have been fully considered but they are not persuasive.

#### As per arguments for claims 1 and 10:

The Applicant states on page 6, third paragraph, "First, the Examiner states that an address table used during the second stage intra-permutation (col. 5, lines 53-55) anticipates the register for updating and registering a plurality of parameters for setting an operating condition of the interleaver recited in Claim 1. However, an address table by definition does not update and register a plurality of parameters, but merely stores addresses". The Examiner respectfully disagrees and asserts that Suda's tables are updated and register a plurality of parameters. In Suda, col. 6, l. 6 to col. 8, l. 51 the tables are formed (updated) from sequences (a plurality of parameters) calculated. It is known in the art that look-up tables are dynamic in nature and are regularly updated and store values.

The Applicant also states "Second, Claim 1 recites an address calculator (an element which the Examiner does not make reference to) for generating a finally interleaved address.... The closest thing to an address calculator in Suda et al. is the address table, and by definition, a table is not a calculator". The Examiner asserts that the address calculator of the instant applicant as recited in claim 1 is equivalent to Suda's interleaver 22 of the turbo encoder, which includes first, second and third stages 41, 42 and 43. The Examiner also asserts that Suda's interleaver 22 teaches the limitations of claim 1 as set forth in the previous office action of record. It is known to one skilled in the art that prior art interleavers, such as interleaver 100 of Applicant's Admitted Prior Art (AAPA) on pages 1-5, calculates inter-row permutation pattern  $T(j)$ , intra-row permutation basic sequence  $s(i)$ , and performs an increment operation.

The Applicant further states "The intra-row permutation 'sequence of Suda et al. is not the intra-row permutation pattern increment arrangement value recited in Claim 1. The Applicant's argument for claim 10 is similar and will be addressed here. Suda et al. does not teach or disclose the intra-row permutation pattern increment management value recited in Claim 1". The Examiner respectfully disagrees and asserts Suda teaches step S1 is to compute a mapping sequence  $c(i)$  for intra-row permutation defined as follows:  $c(i) = (g \cdot o^i) \pmod{P}$  (**the increment arrangement value  $\text{incr}(j)$** ). (Col. 5, l. 65 to col. 6, l. 5). The increment arrangement value, also known in the art as the remainder in a byproduct result of Suda's mapping sequence  $c(i)$  calculation since the mod of the prime number  $P$  results in a remainder the value of the mapping sequence  $c(i)$  has that remainder or increment value. Therefore, the Examiner asserts that Suda

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teaches all the elements of claim 1 and 10 as set forth in the previous office action of record.

It is the Examiner's conclusion that independent claims 1 and 10 are not patentably distinct or non-obvious over the prior arts of record namely, Suda et al. (US-6553516). Therefore, the rejection is maintained. Based on their dependency on independent claims 1 and 10, claims 2-5, 7, and 9 and 11-12, respectively, stand rejected.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5, 7 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Suda et al. (US-6553516), hereinafter Suda.

#### **Claim 1 and 10:**

Suda teaches the interleaver 22 of the turbo encoder includes first, second and third stages 41, 42 and 43. Suda refers to Figure 5 to teach the first stage 41, having a 664-bit input sequence 40, is divided into eight blocks B<sub>1</sub>-B<sub>8</sub>, which are then written into a two-dimensional array (buffer), which consists of 8 rows and 83 columns (**a data**

**storage device for storing data input to the turbo encoder and outputting data corresponding to the address generated by the address calculator).** Suda also teaches in the third stage 43 an inter-permutation is performed in which the order of the rows arranged in the two-dimensional buffer is permuted (**an inter-row permutation pattern  $T(j)$** ). Suda further teaches the intra-permutation at the second stage 42 uses a table created by the steps S1-S7 as an address table (**a register for updating and registering a plurality of parameters for setting an operating condition of the interleaver**), and processes input data written into the two-dimensional buffer (data storage) by referring to the address table. Suda discloses that step S1 is to compute a mapping sequence  $c(i)$  for intra-row permutation (**an intra-row permutation pattern increment arrangement value  $incr(j)$** ). Suda also discloses after the first through third stages are performed, data is read from the two-dimensional buffer (data storage) in the longitudinal direction (column direction) at step 110 shown in FIG. 10, whereby an interleaved coded sequence 44 can be obtained. (Col. 5, l.15 to col. 6, l. 5, Fig. 5).

Claims 2 and 11:

**“an intra-row permutation pattern generator for calculating an intra-row permutation pattern value using the intra-row permutation pattern increment arrangement value  $incr(j)$ ”**

This limitation is rejected as per claim 1 (intra-permutation at the second stage 42).

**“an intra-row permutation pattern storage arrangement device for storing intermediate data while the intra-row permutation pattern generator calculates the intra-row permutation pattern”**

Suda teaches the numbers defined in the sequence permutation table t0 indicate the bit allocations after permutation where, as shown in FIG. 7B, the sequence permutation table t0 includes the one-dimensional sequence (pattern) starting from the left uppermost position. (Col. 6, ll. 26-35).

**“a final address generator for calculating an address of finally interleaved data using the inter-row permutation pattern T(j) from the register and the intra-row permutation basic sequence s(i) corresponding to the intra-row permutation pattern value generated by the intra-row permutation pattern generator”**

This limitation is rejected as per claim 1 (Suda also discloses after the first through third stages are performed...).

Claim 3:

**“the register updates and registers parameters used to calculate inter-row/intra-row permutation pattern of the input data to be interleaved, and provides the parameters to an intra-row permutation pattern generator of the address calculator to generate an intra-row permutation pattern for generating an interleaved final intra-row permutation pattern”**

This limitation is rejected as per claim 1 (Suda further teaches the intra-permutation at the second stage 42 uses a table created by the steps S1-S7 as an address table ...).

Claim 4:

**“a parameter  $K$  indicating a number of input data bits”**

Suda teaches the number of bits input to the turbo encoder is  $N_{IN}$  (which corresponds to  $K$  in FIG. 3). (Col. 4, ll. 38-41).

**“a parameter  $\mu$  indicating a primitive root”**

Suda teaches step S1 is to obtain the primitive root  $g_0$  of the Galois field of the characteristic  $P$  (which corresponds to the number of columns (a parameter  $C$  indicating a number of columns of the input data) and is equal to 83 in the case shown in FIG. 5) at step 105 shown in FIG. 10... (Col. 5, l. 57 to col. 6, l. 5).

**“a parameter  $p$  indicating a prime number”**

Suda teaches At step (2), the prime number  $P$  that is greater than  $n$  and closest to  $n$  is obtained. (Col. 4, ll. 42-48).

**“a parameter  $R$  indicating a number of rows of the input data”**

Suda teaches step S2 corresponds to a case when a parameter  $I$  indicative of the row number is set equal to 1 at step 106 shown in FIG. 10. (Col. 6, ll. 36-36).

Claim 5:

**“the intra-row permutation pattern generator uses an inter-row inverse permutation pattern  $TI(j)$  determined by inversing the inter-row permutation pattern  $T(j)$  to calculate a permuted prime integer sequence  $r(j)$  for calculating a final intra-row permutation pattern  $U^j(i)$ ”**



Suda teaches, as shown in FIG. 1C, a turbo decoder is made up to two decoders 1 and 2, two interleavers 3 and 4, and a deinterleaver 5. (Col. 1, ll. 40-42, col. 8, ll. 39-42, col. 9, ll. 13-15, 49-55).

Claim 7:

Suda teaches step S1 is to compute a mapping sequence  $c(i)$  for intra-row permutation defined as follows:  $c(i) = (g_0^i) \pmod{P}$  (**the increment arrangement value  $incr(j)$** ). (Col. 5, l. 65 to col. 6, l. 5).

Claims 9 and 12:

Suda teaches the data is input sequentially to the data storage device (input sequence 40, Fig. 5).

***Allowable Subject Matter***

5. The following is an Examiner's Statement of Reasons for Allowance:

The prior arts of record teach an interleaver for a turbo encoder with a register for updating and registering a plurality of parameters for setting an operating condition of the interleaver. The prior arts of record also teach an address calculator for generating a finally interleaved address using an inter-row permutation pattern, an intra-row permutation pattern increment arrangement value and an intra-row permutation basic sequence provided from the register. The prior arts of record further teach a data storage device for storing data input to the turbo encoder and outputting data corresponding to the address generated by the address calculator; Suda et al. (US-6553516) is one example of such prior arts. The prior arts of record, however, fail to

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teach, singly or in combination, an intra-row permutation pattern generator which comprises the details disclosed in claim 6, namely, a first adder and a second adder, a first multiplexer, a sign detector connected to the second adder and the first multiplexer, a second multiplexer.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

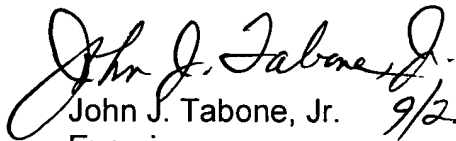
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

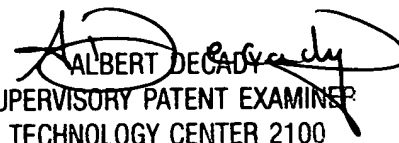
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
John J. Tabone, Jr. 9/29/05  
Examiner  
Art Unit 2133

  
ALBERT DECADY  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100